FIG.1

DELAY CIRCUIT ACCORDING TO THE FIRST EMBODIMENT

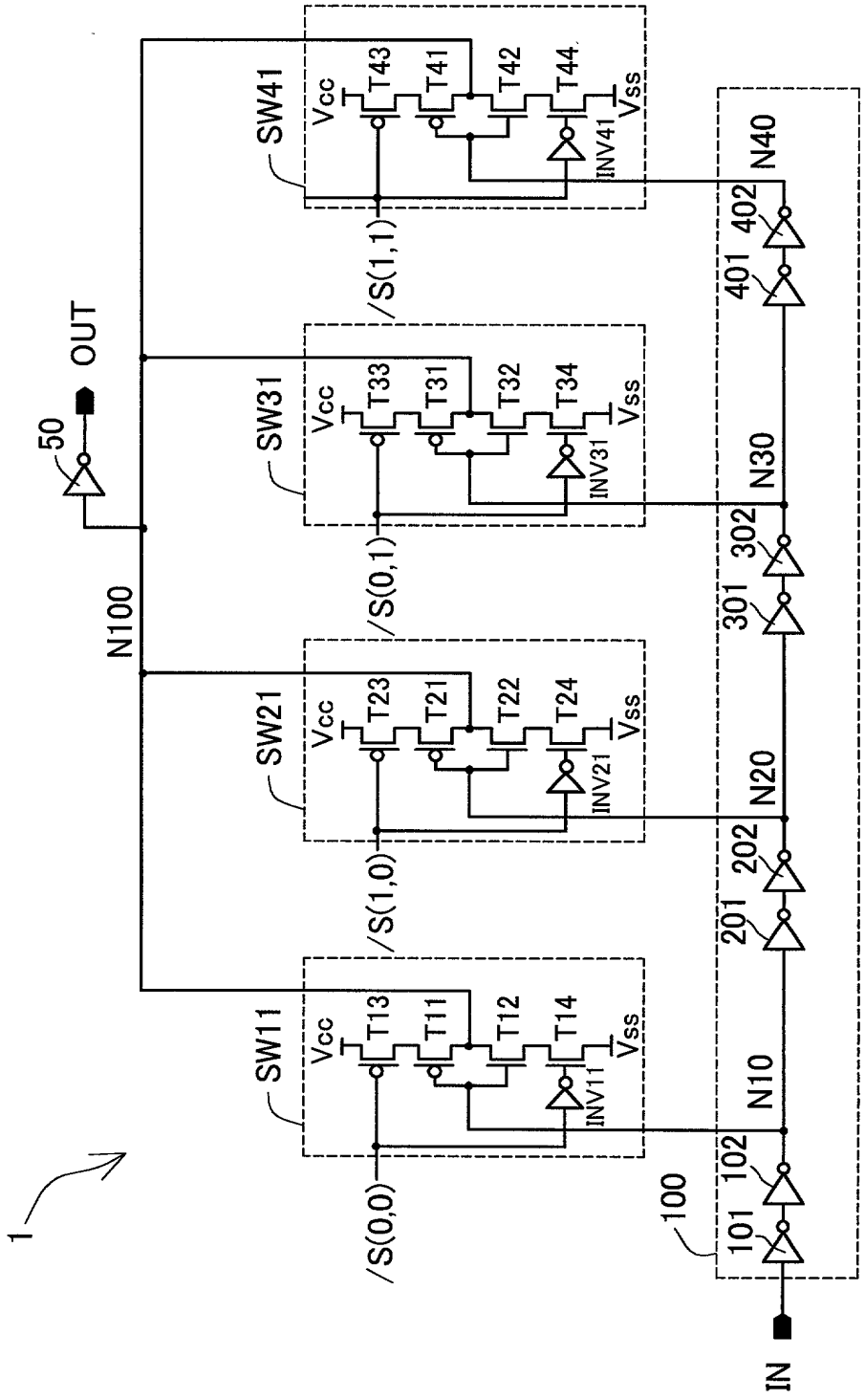

FIG.2

DELAY CIRCUIT ACCORDING TO THE SECOND EMBODIMENT

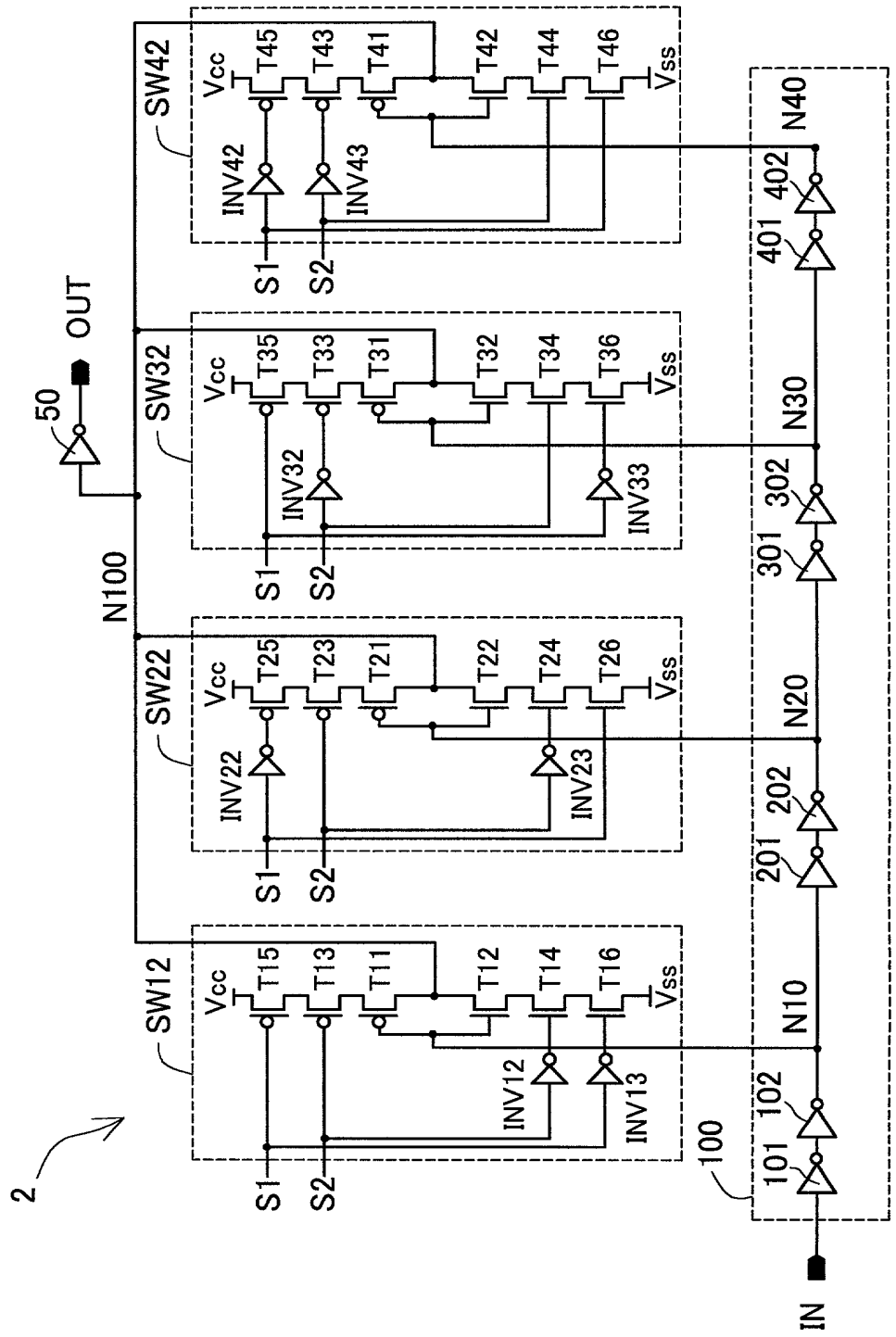

FIG.3

DELAY CIRCUIT ACCORDING TO THE THIRD EMBODIMENT

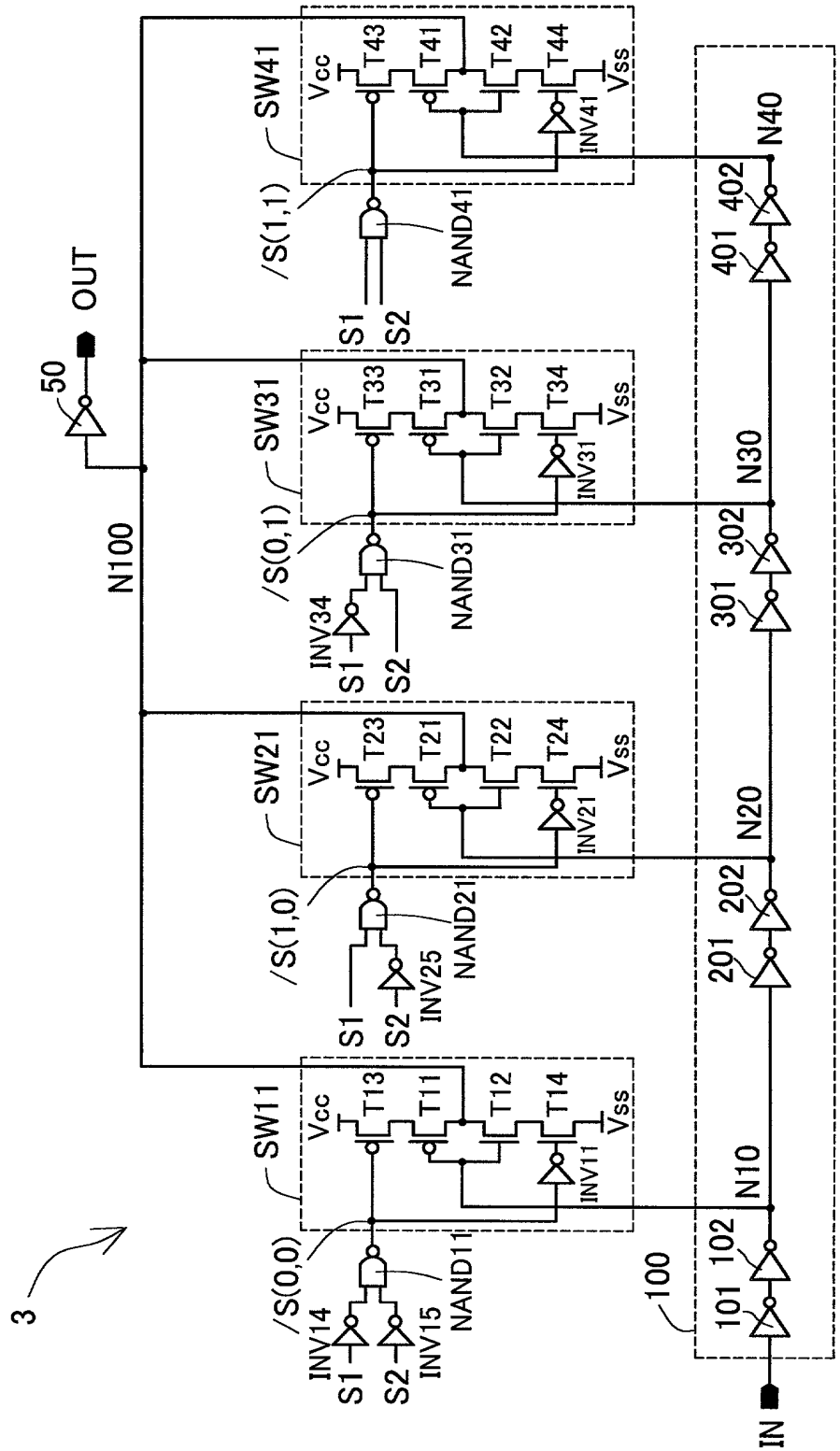

FIG.4

DELAY CIRCUIT ACCORDING TO THE FOURTH EMBODIMENT

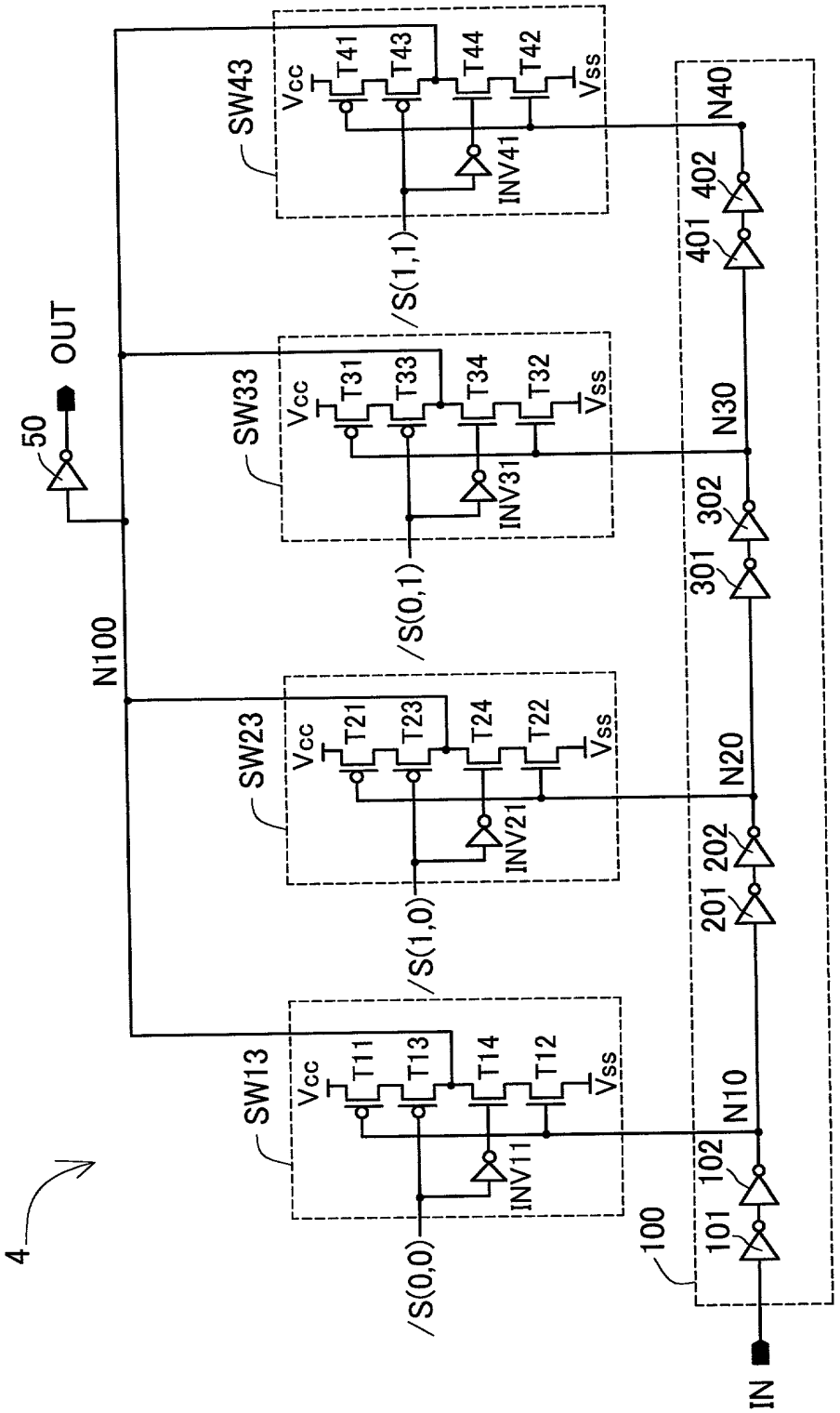

FIG.5

DELAY CIRCUIT ACCORDING TO THE FIFTH EMBODIMENT

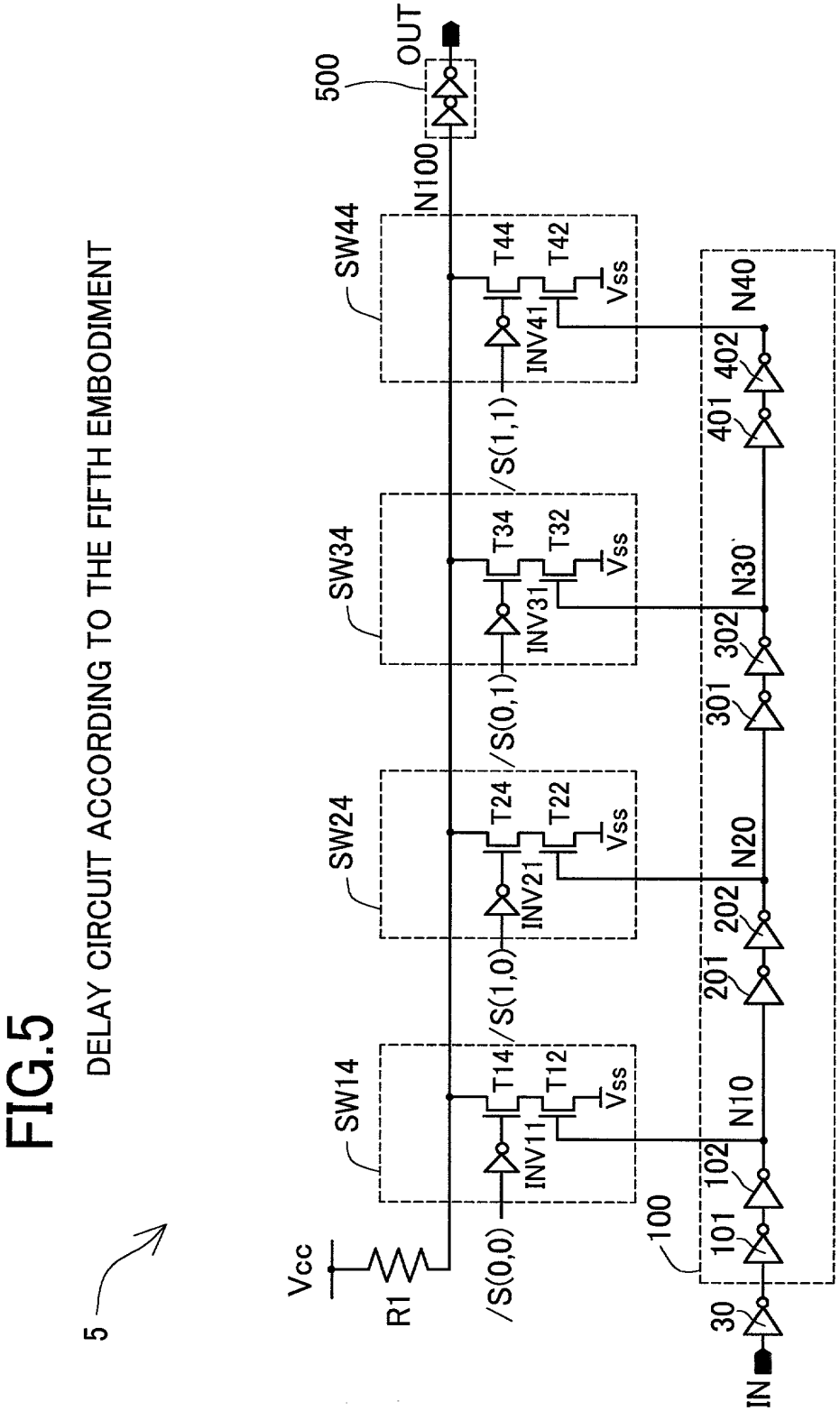

FIG.6

DELAY CIRCUIT ACCORDING TO THE SIXTH EMBODIMENT

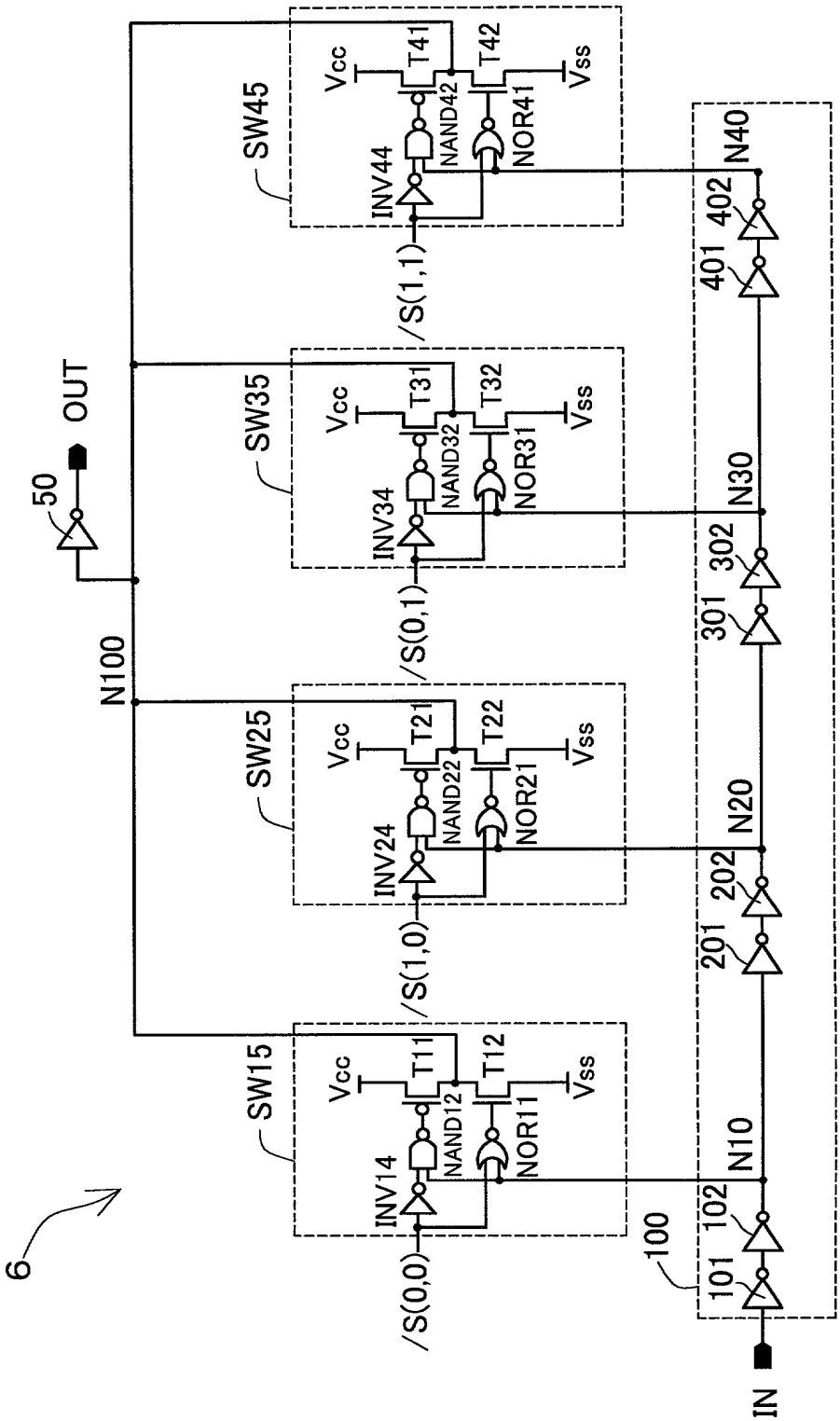

FIG.7

DELAY CIRCUIT ACCORDING TO THE SEVENTH EMBODIMENT

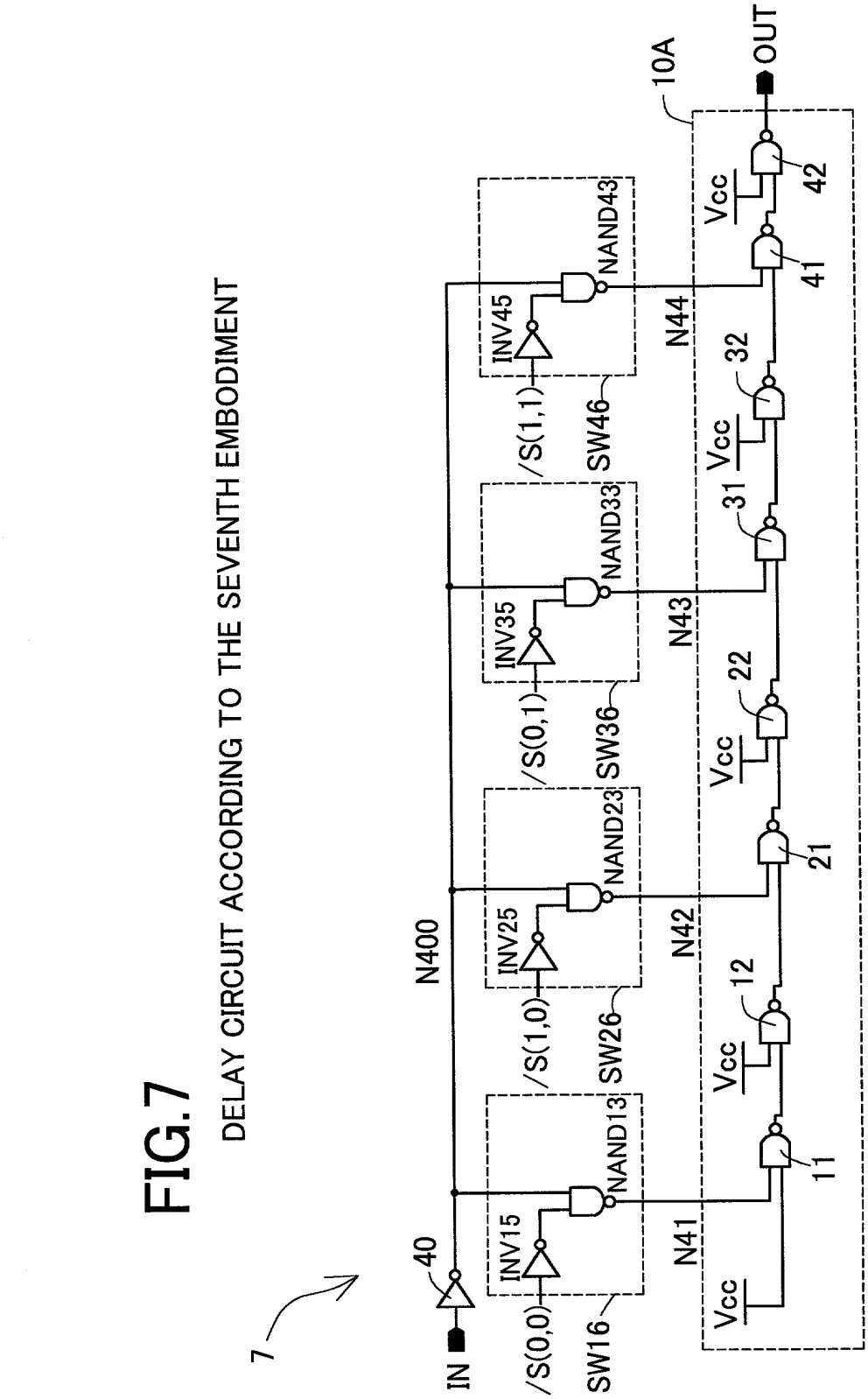

FIG.8 PRIOR ART

FIRST DELAY CIRCUIT OF THE FIRST RELATED TECHNOLOGY

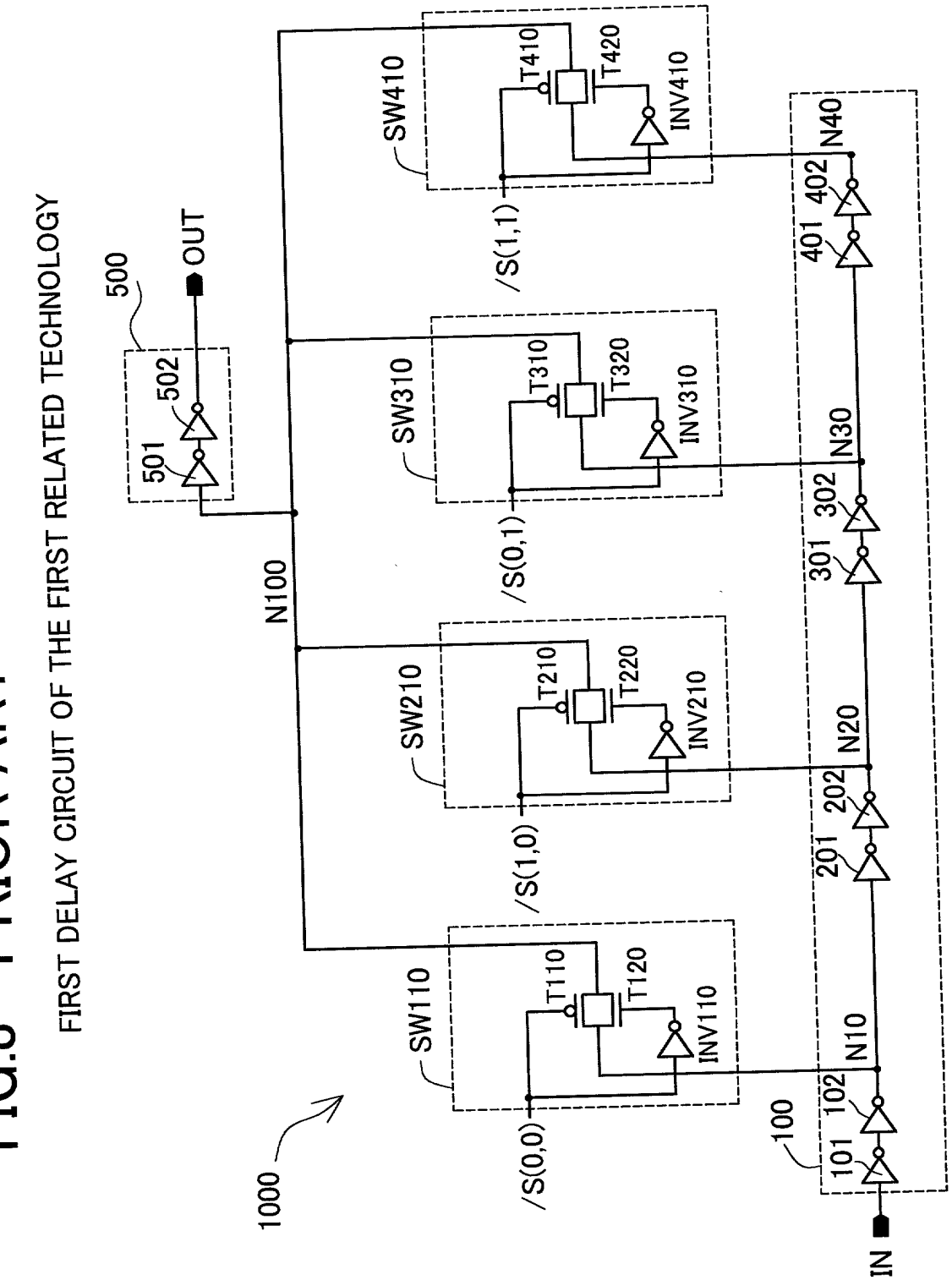

FIG.9 PRIOR ART

SECOND DELAY CIRCUIT OF THE SECOND RELATED TECHNOLOGY

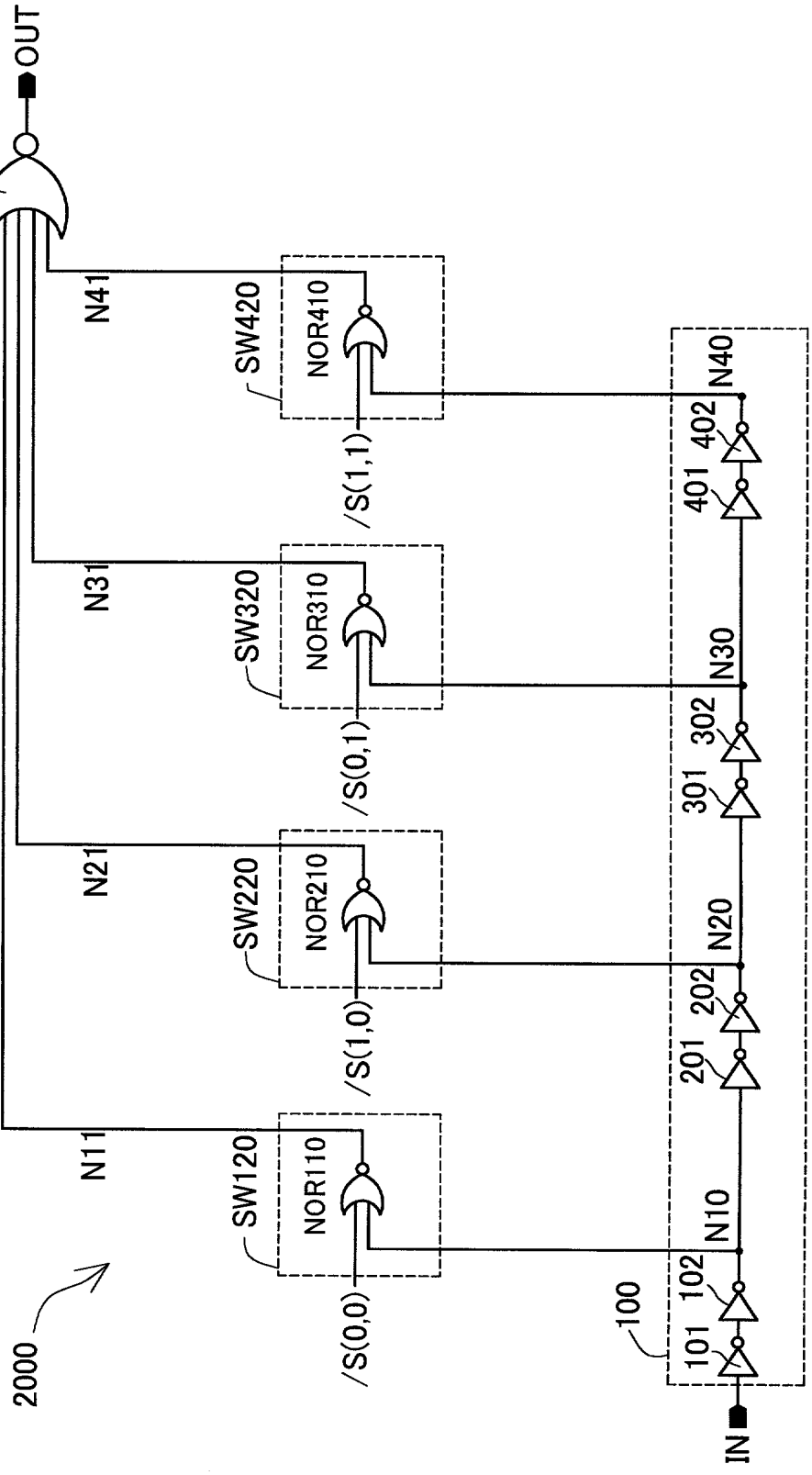

FIG.10 PRIOR ART

THIRD DELAY CIRCUIT OF THE THIRD RELATED TECHNOLOGY